SGS-THOMSON MICROELECTRONICS

TS68952

MODEM TRANSMIT/RECEIVE CLOCK GENERATOR

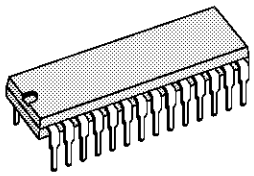
- INDEPENDANT TRANSMIT AND RECEIVE CLOCK GENERATORS WITH DIGITAL PHASE LOCKED LOOPS
- TRANSMIT DPLL SYNCHRONIZATION ON EXTERNAL TERMINAL CLOCK OR INTERNAL RECEIVE CLOCK
- RECEIVE DPLL SYNCHRONIZATION CONTROLLED FROM THE BUS
- FOUR EXTERNAL CLOCKS AVAILABLE, PLESIOCHRONOUS ON TRANSMIT AND RECEIVE CHANNELS :
  - BIT RATE CLOCK
  - BAUD RATE CLOCK
  - SAMPLING CLOCK
  - MULTIPLEXING CLOCK
- DIRECT INTERFACE WITH STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE

DESCRIPTION

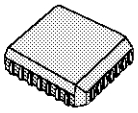
The TS68952 is a Clock Generator circuit designed to generate all the necessary clocks frequencies needed by high-speed modems applications.

The TS68952 copes with all the CCITT recommendations from V.22 to V.33 including full-duplex recommendations. Used in conjunction with the TS68950 Transmit (Tx) Analog Front-End circuit and the TS68951 Receive Analog Front-End*, it provides a very cheap and efficient interface to digital signal processing functions in high speed modems.

* The interconnection between the 3 chips of the Modem Analog Front-end (MAFE) and a DSP is described page 11.



DIP28
(Plastic Package)
ORDER CODE : TS68952CP



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PIN CONNECTIONS

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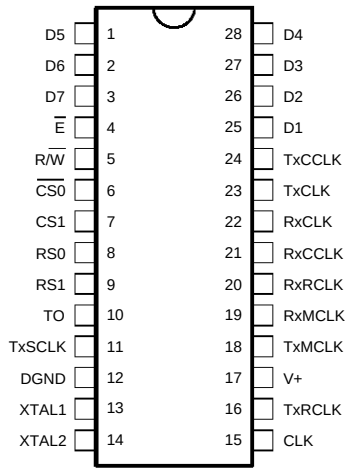

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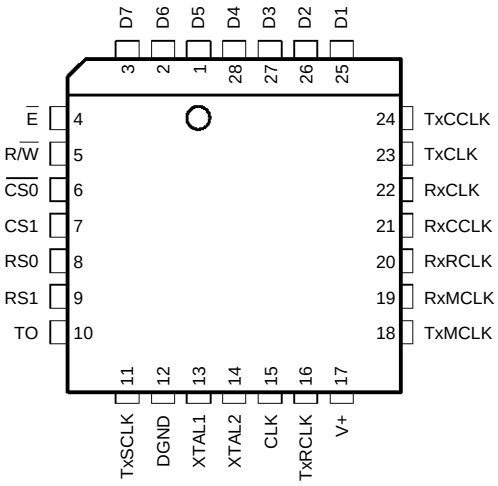


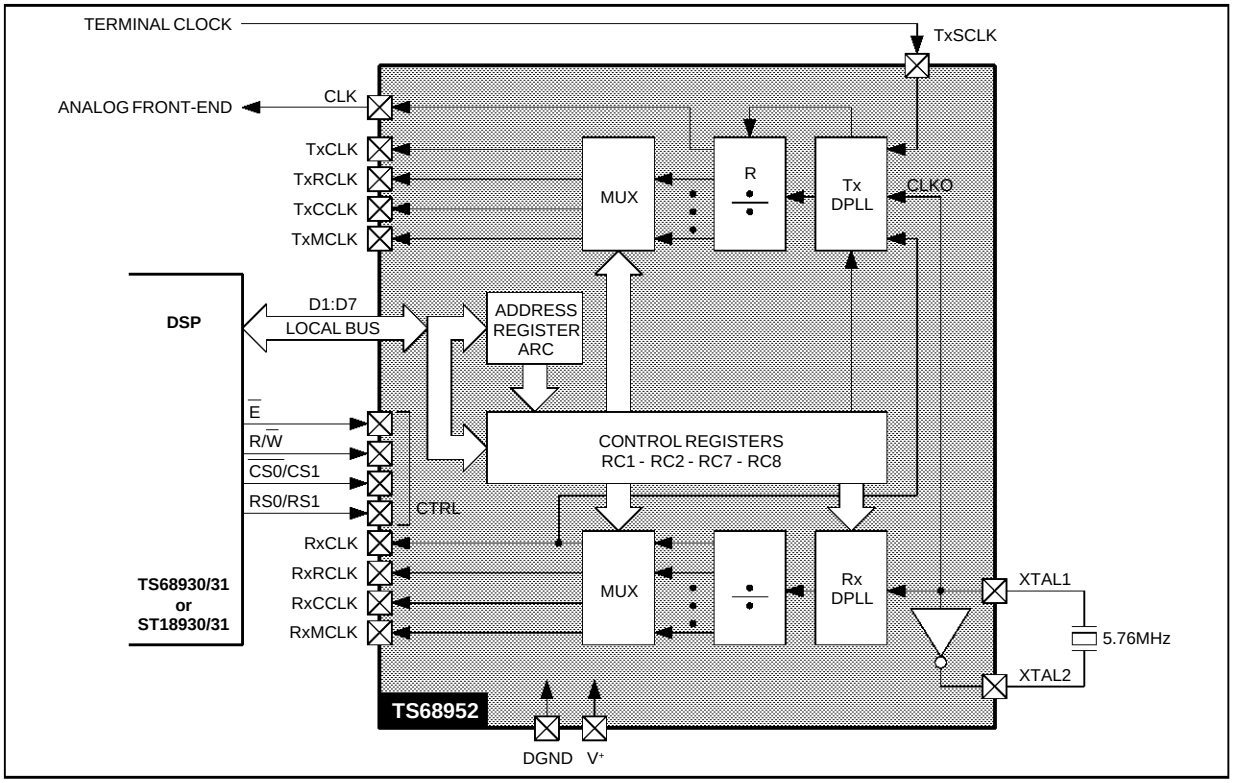
68952-01.EPS / 68952-02.EPS

PIN FUNCTIONS

Pin N°	Name	Function
25 - 26 27 - 28 - 1 2 - 3	D1-D7	Data Bus Inputs to Internal Registers (DO is not used)
4	$\overline{E}$	Enable Input. Data are strobed on the positive transitions of this input.
5	R/$\overline{W}$	Read/Write Selection Input. Internal registers can be written when R/W = 0. Reading mode is only used for Rx analog front-end chip.
6 - 7	$\overline{CS0}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1
8 - 9	RS0-RS1	Register Select Inputs. Used to select address or control registers.
10	TO	Test Output. Must be left open.
11	TxSCLK	Transmit Synchronizing Clock Input. Normally tied to an external terminal clock. When this pin is tied to a permanent logical level, transmit DPLL free-runs or can be synchronized to the receive clock system.
12	DGND	Digital Ground = 0V All digital signals are referenced to this pin.
13	XTAL1	Crystal Oscillator or Pulse Generator Input
14	XTAL2	Crystal Oscillator Output
15	CLK	1.44MHz Clock output useful for Tx and Rx analog front-end chips
16	TxRCLK	Transmit Baud Rate Clock Output
17	V^+	Positive Power Supply Voltage = +5V ±5%
18	TxMCLK	Transmit Multiplexing Clock Output
19	RxMCLK	Receive Multiplexing Clock Output
20	RxRCLK	Receive Baud Rade Clock Output
21	RxCCLK	Receive Conversion Clock Output
22	RxCLK	Receive Bit Rate Clock Output
23	TxCLK	Transmit Bit Rate Clock Output
24	TxCCLK	Transmit Conversion Clock Output

68952-01.TBL

BLOCK DIAGRAM



68952-03.EPS

FUNCTIONAL DESCRIPTION

The TS68952 is a digital circuit that synthesises all the frequencies required to implement synchronous voice-grade MODEMs from 1200bps to 19200bps. It consists of two clock generators using Digital Phase Locked Loops (DPLLs). Frequency programming and DPLL updating can be obtained through four control registers accessed by indirect or cyclical addressing (see p 8117).

This circuit is a part of a three chip Modem Analog Front-End that also includes the TS68950 transmit analog interface and the TS68951 receive analog interface.

POWER-UP INITIAL CONDITIONS

Following power-up, the eight transmit and receive clock outputs are undefined and may deliver any frequencies. Control registers RC1 and RC2 must be properly programmed to obtain the requested operation.

CLOCK GENERATION

Master clock is obtained from either a crystal tied between XTAL1 and XTAL2 pins or an external signal connected to the XTAL1 pin ; in this case, the XTAL2 pin should be left open. Clock frequency nominal value is 5.76MHz, but 5.12MHz and 5.40MHz frequencies are also specified for particular applications.

The different transmit (Tx) and receive (Rx) clocks are obtained by frequency division in several counters and output selection through digital multiplexers. They can be synchronized on external signal via two independent digital phase locked loops (DPLL).

TRANSMIT DPLL

As shown Figure 1, the TxDPLL operates by adding or subtracting pulses to a 2.88MHz internal clock, with a reference frequency that is a submultiple of the programmed "rate clock" frequency. This corresponds to phase leads or phase lags of about 350ns duration, more precisely, two master clock periods.

The TxDPLL can be synchronized on an external terminal clock tied to TxSCLK pin or on the receive bit clock RxCLK internally generated from the RxDPLL. It can also free-run without any phase shift, when the TxSCLK input is tied to a fixed logical level.

TRANSMIT CLOCKS

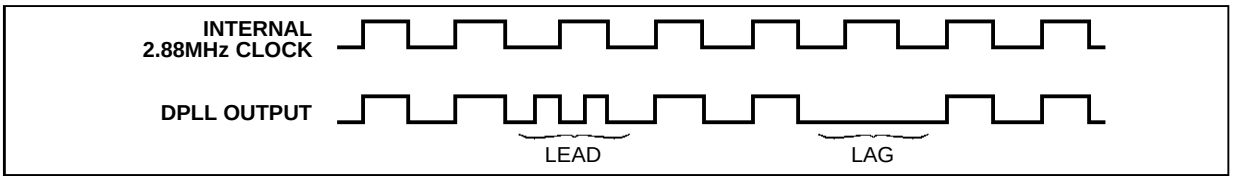
The TS68952 delivers four synchronous Tx clocks :
- a bit clock, TxCLK, whose frequency equals the bit rate ot the modem,
- a baud clock, TxRCLK, whose frequency equals the baud rate of the modem,
- a conversion clock, TxCCLK, that gives the sampling frequency of the Tx converter (also used by the Rx converter in echo cancelling applications),
- a multiplexing clock, TxMCLK, usable when several terminals are multiplexed on a single physical link.

The frequencies of these four clocks are programmable through RC1 and RC2 control registers. Their cyclical ratio is exactly 1 : 2, except for the 16.8kHz frequency whose cyclical ratio is slightly modulated around 1 : 2, and their relative phase locking is ensured without user intervention, by periodic reset of the counters.

Immediate phasing of these clocks on the synchronizing external TxSCLK or internal RxCLK clock can be obtained through bit 7 or RC8 register. The content of this register is automatically cleared after phasing completion.

The TS68952 also delivers, on pin CLK, a 1.44MHz clock that is synchronous with the Tx clock system and will be used as the main clock to the TS68950/51 analog interface circuits.

Figure 1 : DPLL Lead and Lag



RECEIVE DPLL

RxDPLL phase shifts are performed by addition and subtraction of pulses from an internal 1.44MHz clock under the control of RC8 register. Two modes of operation are provided :

- a coarse phase lag whose amplitude has been loaded into RC7 register, can be controlled by one bit of RC8 register. This mode is useful for a fast synchronization of the RxDPLL. The phase lag is obtained by suppressing a variable number of pulses at the input of the counters,
- a fine phase shift with lead or lag amplitude equal to two master clock periods, can be controlled by two bits of RC8. This mode corresponds to normal operation. The phase shifts are obtained by addition or suppression of pulses as indicated in Figure 1.

RC8 register is automatically cleared when the programmed phase shift is completed. Simultaneous programming of Tx and Rx control bits of this register has to be avoided.

RECEIVE CLOCKS

The TS68952 delivers four Rx clocks with the same nominal frequency values as their Tx counterparts :

- a bit clock RxCLK,
- a baud clock RxRCLK,
- a conversion clock RxCCLK,
- a multiplexing clock RxMCLK.

The Rx and Tx output clocks are plesiochronous.

BIT CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC1 Register							Output Frequency (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76MHz	F_Q = 5.40MHz	F_Q = 5.12MHz
0	0	0	0				19.2		
0	0	0	1				16.8		
0	0	1	0				14.4		
0	0	1	1				12.0		
0	1	0	0				9.6		
0	1	0	1				7.2		6.4
0	1	1	1				6.4		
1	0	0	0				6.0		
1	0	0	1				4.8		
1	0	1	0				3.2	3.0	
1	0	1	1				2.4		
1	1	0	0				1.2		
1	1	0	0				0.6		
1	1	0	1				0.6		
1	1	1	0				0.6		
1	1	1	1				0.6		

68952-02.TBL

F_Q = crystal oscillator frequency.

RATE CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC1 Register							Output Frequency (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
				0	0	0	2.4		2.133
				0	0	1	2.0*		
				0	1	0	1.6**	1.5	
				0	1	1	1.2		
				1	0	0	0.6		
				1	0	1	0.6		
				1	1	0	0.6		
				1	1	1	0.6		

68952-03.TBL

Note : Phase shift frequency of TxDPLL is 600Hz excepted for (*) 1000Hz and for (**) 800Hz.

CONVERSION CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC2 Register							Output Frequency (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HM3	HM2	HM1	HS2	HS1	HTHR	—	F_Q = 5.76MHz	F_Q = 5.40MHz	F_Q = 5.12MHz
			0	0			9.6	9.0	8.533
			0	1			8.0	7.5	
			1	0			7.2		
			1	1			7.2		

68952-04.TBL

MULTIPLEXING CLOCK FREQUENCY PROGRAMMING (Tx and Rx)

RC2 Register							Output Frequency (kHz)
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	—	F_Q = 5.76 MHz
0	0	0					1440
0	0	1					288
0	1	0					12
0	1	1					9.6
1	0	0					7.2
1	0	1					4.8
1	1	0					2.4
1	1	1					1.2

68952-05.TBL

Tx SYNCHRONIZATION SIGNAL PROGRAMMING

RC2 Register							Synchronization Signal
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	—	
					0		RxCLK
					1		TxSCLK (note 1)

68952-06.TBL

Note : 1.TxDPLL free-runs if there is no transition on this input.

TxCLOCK GENERAL RESET

RC8 Register (notes 1, 2)							
D7	D6	D5	D4	D3	D2	D1	The Tx counters are resetted on the first negative-going transition of the synchronization signal following MPE programming to 1.
MPE	SPR	AVRE	VAL	INIT	–	–	
1	0	0	0	0			Next Negative-Going Transition on Synchronization Signal.

68952-07.TBL

RxCLOCK PHASE SHIFT PROGRAMMING

RC8 Register (note 1)							Action on RxDPLL
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	INIT	-	-	
0	1	0	0	0			Phase Lag of Programmed Amplitude
0	0	0	1	0			Phase Lag of Two 5.76MHz Master Clock Periods
0	0	1	1	0			Phase Lead of Two 5.76MHz Master Clock Periods

68952-08.TBL

Notes : 1. RC8 register is cleared after the programmed control operation is completed.
2. INIT bit is only used for test purpose.

RxCLOCK PHASE SHIFT AMPLITUDE PROGRAMMING

RC7 Register							Phase Shift in Degrees		Number of Master Clock Pulses Suppressed
D7	D6	D5	D4	D3	D2	D1			
SP5	SP4	SP3	SP2	SP1	-	-	1200 Bauds*	1600 Bauds	
0	0	0	0	0			1.5	2	20
0	0	0	0	1			3	4	40
0	0	0	1	0			4.5	6	60
0	0	0	1	1			6	8	80
0	0	1	0	0			7.5	10	100
0	0	1	0	1			9	12	120
0	0	1	1	0			10.5	14	140
0	0	1	1	1			12	16	160
0	1	0	0	0			13.5	18	180
0	1	0	0	1			15	20	200
0	1	0	1	0			16.5	22	220
0	1	0	1	1			18	24	240
0	1	1	0	0			19.5	26	260
0	1	1	0	1			21	28	280
0	1	1	1	0			22.5	30	300
0	1	1	1	1			24	32	320
1	0	0	0	0			22.5	30	300
1	0	0	0	1			45	60	600
1	0	0	1	0			67.5	90	900
1	0	0	1	1			90	120	1200
1	0	1	0	0			112.5	150	1500
1	0	1	0	1			135	180	1800
1	0	1	1	0			157.5	210	2100
1	0	1	1	1			180	240	2400
1	1	0	0	0			202.5	270	2700
1	1	0	0	1			225	300	3000
1	1	0	1	0			247.5	330	3300
1	1	0	1	1			270	360	3600
1	1	1	0	0			292.5		3900
1	1	1	0	1			315		4200
1	1	1	1	0			337.5		4500
1	1	1	1	1			360		4800

68952-09.TBL

(*) 2400 bauds : multiply by two. 600 bauds : divide by two.

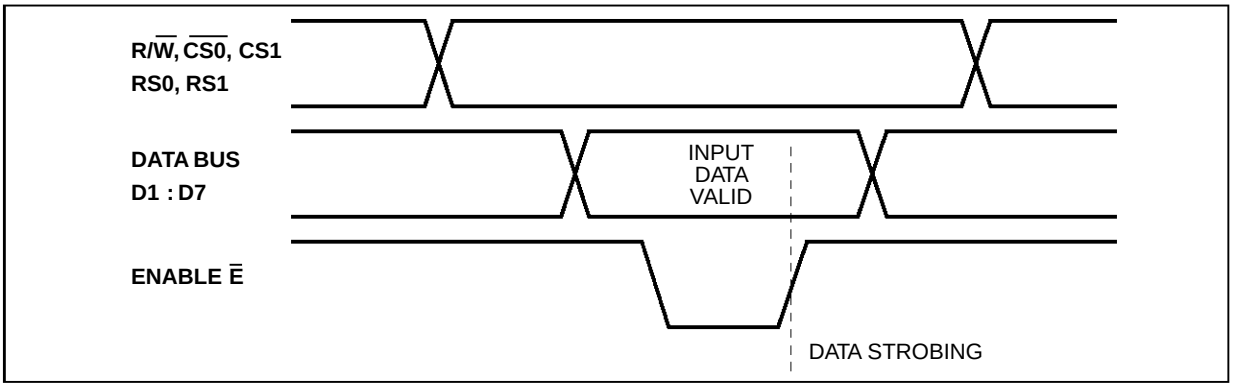
DATA BUS CONTROL

Six signals control the access from the bus to the internal registers according to the table and the timing diagram given below. Control registers are written using an indirect addressing mode where the internal address is stored in the 3 bit ARC register. After each write operation to a control register, the ARC register value is automatically increased by one. This allows cyclical addressing of the eight registers of the MODEM chip set.

R/$\overline{W}$	$\overline{CS0}$	CS1	RS0	RS1	$\overline{E}$	Accessed Register
0	0	1	1	0	⎽↑	Address Register ARC
0	0	1	1	1	⎽↑	Control Register whose Address is in ARC

68952-10.TBL

Figure 2 : Bus Timing Diagram



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DATA FORMAT

Data Loaded in ARC			Addressed Register
D7	D6	D5	
ARC3	ARC2	ARC1	
0	0	0	RC1
0	0	1	RC2
1	1	0	RC7
1	1	1	RC8

68952-11.TBL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	V^+ Supply Voltage to DGND Ground	-0.3, 7	V
	Voltage at any Input or Output	DGND -0.3, V^+ +0.3	V
	Current at any Output	-20, 20	mA
P_{tot}	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, 70	°C
T_{stg}	Storage Temperature	-65, +150	°C

68952-12.TBL

OPERATING RANGE

Ambient Temperature	V^+	DGND
0 °C ≤ T_{amb} ≤ 70 °C	-5.0V ±5%	0V

68952-13.TBL

ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, Electrical Characteristics are specified over the operating range.
Typical values are given for V^+ = 5.0V and T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
POWER DISSIPATION						
I^+	Positive Supply Current				5.0	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2.2			V
I_{IL}	Input Low Level Current	DGND ≤ V_I ≤ $V_{IL\ max}$	-10		10	µA
I_{IH}	Input High Level Current	$V_{IH\ min}$ ≤ V_I ≤ V^+	-10		10	µA
V_{OL}	Output Low Level Current	I_O = 2.5mA			0.4	V
V_{OH}	Output High Level Current	I_O = -2.5mA	2.4			V
CRYSTAL OSCILLATOR INTERFACE						
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5			V
I_{IL}	Input Low Level Curent	DGND ≤ V_I ≤ $V_{IL\ max}$	-15			µA
I_{IH}	Input High Level Current	$V_{IH\ min}$ ≤ V_I ≤ V^+			15	µA

68952-14.TBL

TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DATA BUS ACCESS (Figure 3)						
t_{SCE}	Control Signals Set-up Time	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	40			ns
t_{HCE}	Control Signals Hold Time	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	10			ns
t_{SDI}	Data-in Set-up Time	D1 : D7 to $\overline{E}$	120			ns
t_{HDI}	Data-in Hold Time	D1 : D7 to $\overline{E}$	10			ns
t_{WE}	Enable Signal Low Level Width	$\overline{E}$		180		ns
CLOCK WAVE FORMS (Figure 4)						
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL = 50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL = 50 pF			100	ns

68952-15.TBL

Figure 3 : Data Bus Access

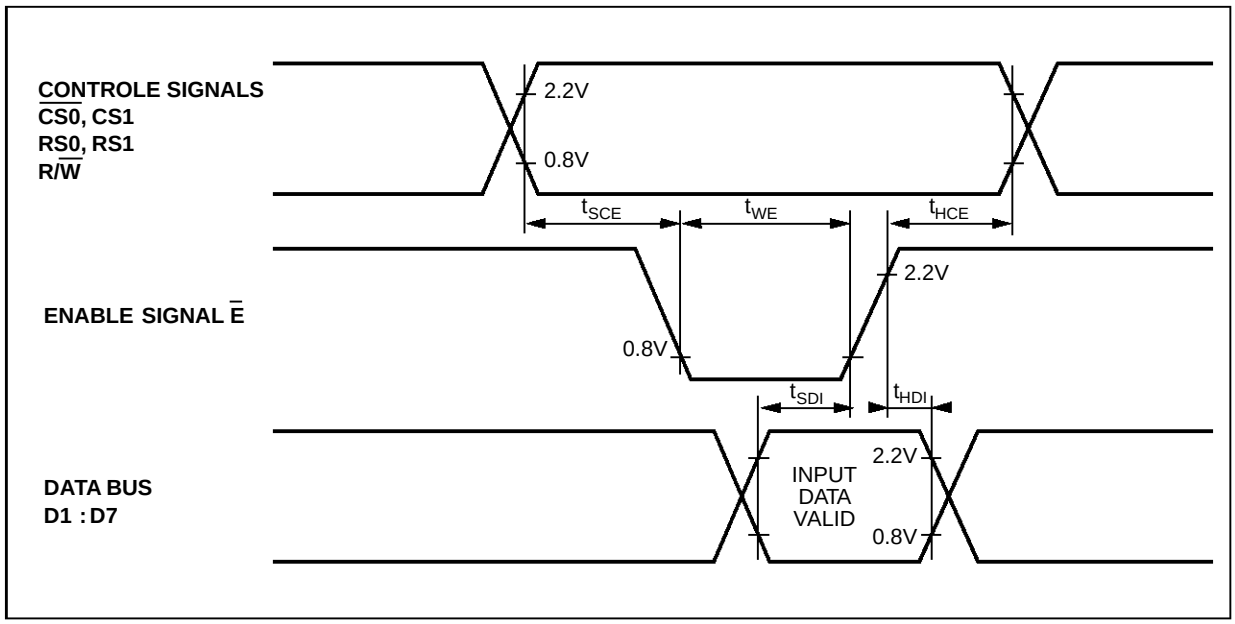
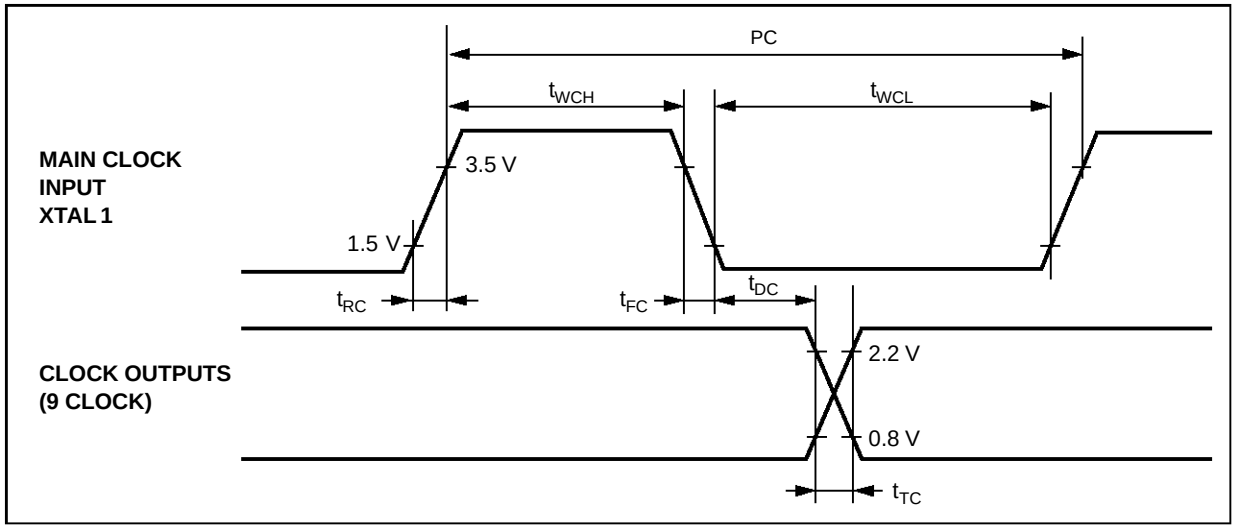
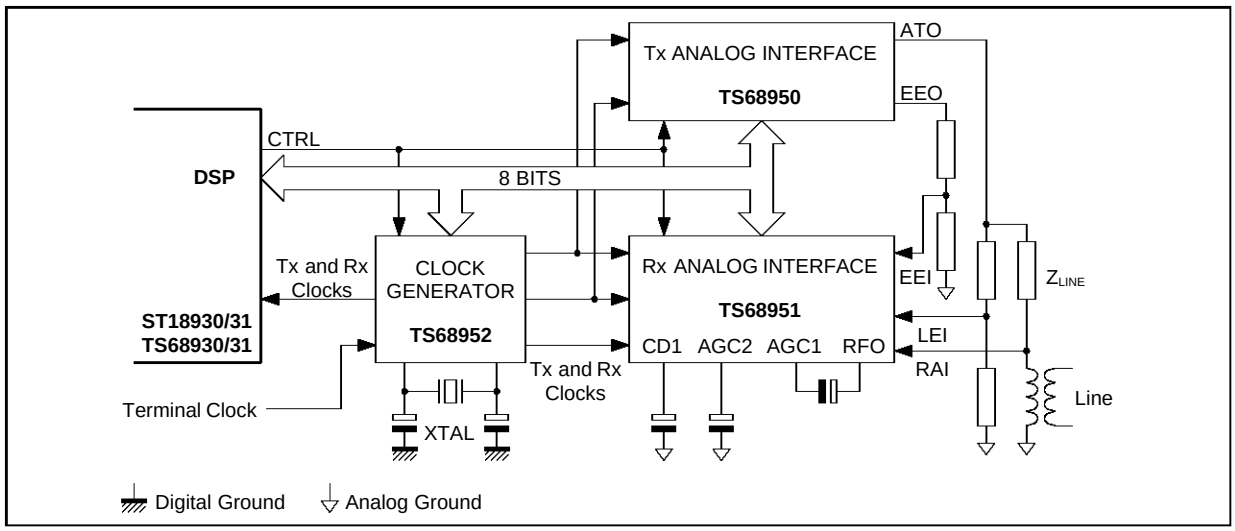


Figure 4 : Clock Wave Forms

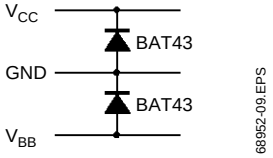


APPLICATION INFORMATION

MODEM ANALOG FRONT-END CHIP SET (TS38950/51/52)

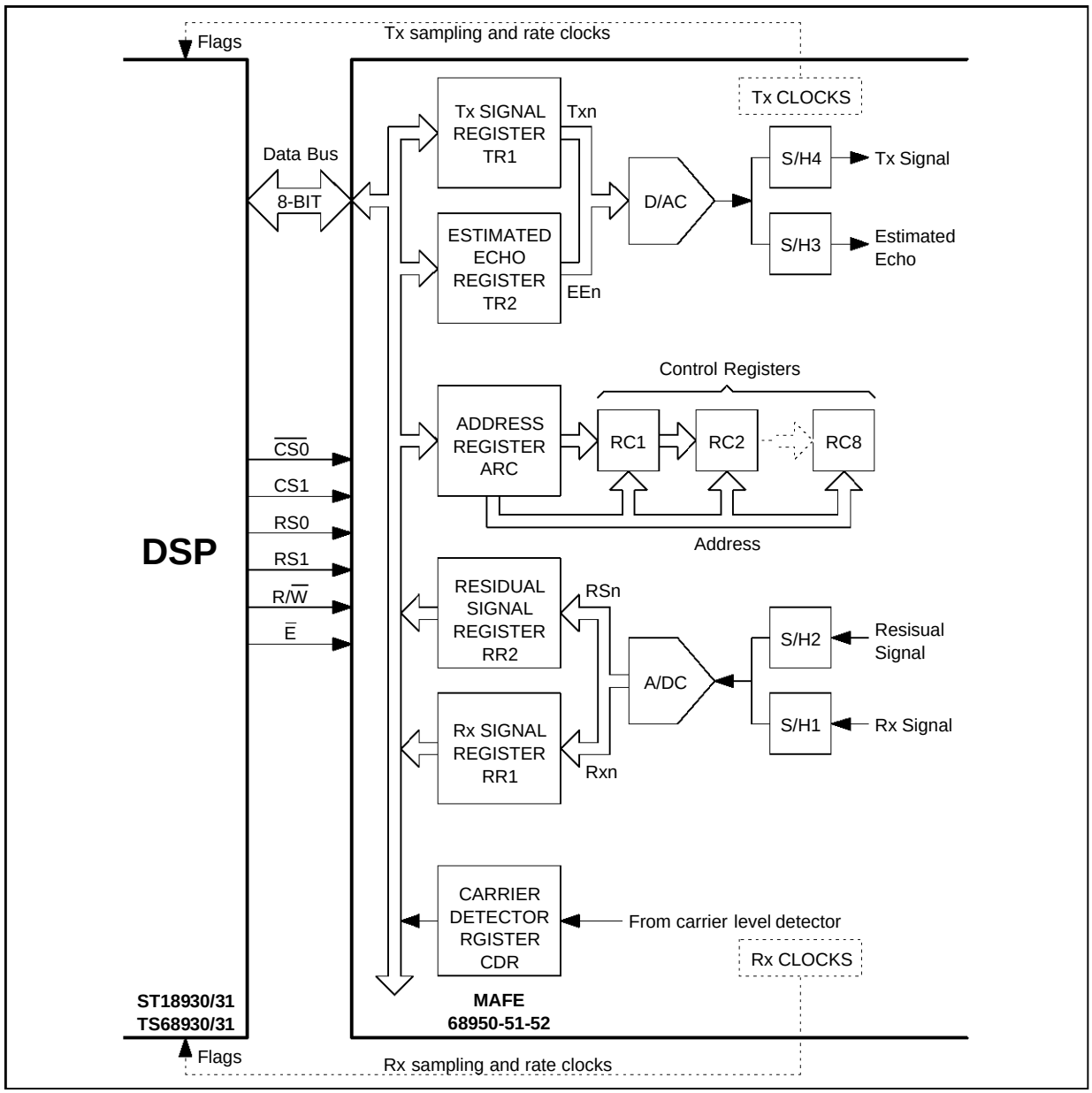


Note : In some cases, external-user circuitry may induce power-up sequency latch-up problems that can be efficiently avoided using ST BAT43 Schottky small signal diodes as follow :



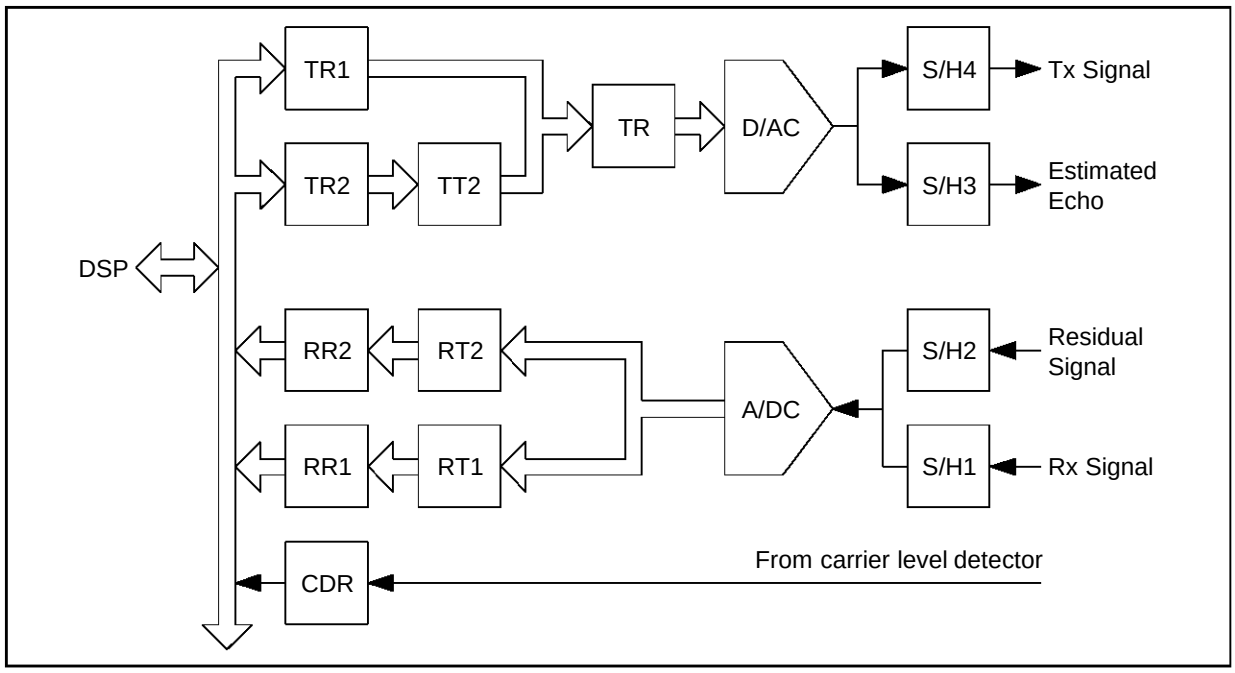
APPENDIX 1

INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/51/52)



APPENDIX 2

DETAILED INPUT/OUTPUT REGISTERS DIAGRAM



68952-11.EPS

	R/$\overline{W}$	RS0	RS1	Register Accessed
Writing	0	0	0	TR1
	0	0	1	TR2
	0	1	0	ARC
	0	1	1	Control Register Addressed by ARC
Reading	1	0	0	RR1
	1	0	1	RR2
	1	1	0	CDR
	1	1	1	Not Used

68952-16.TBL

APPENDIX 3

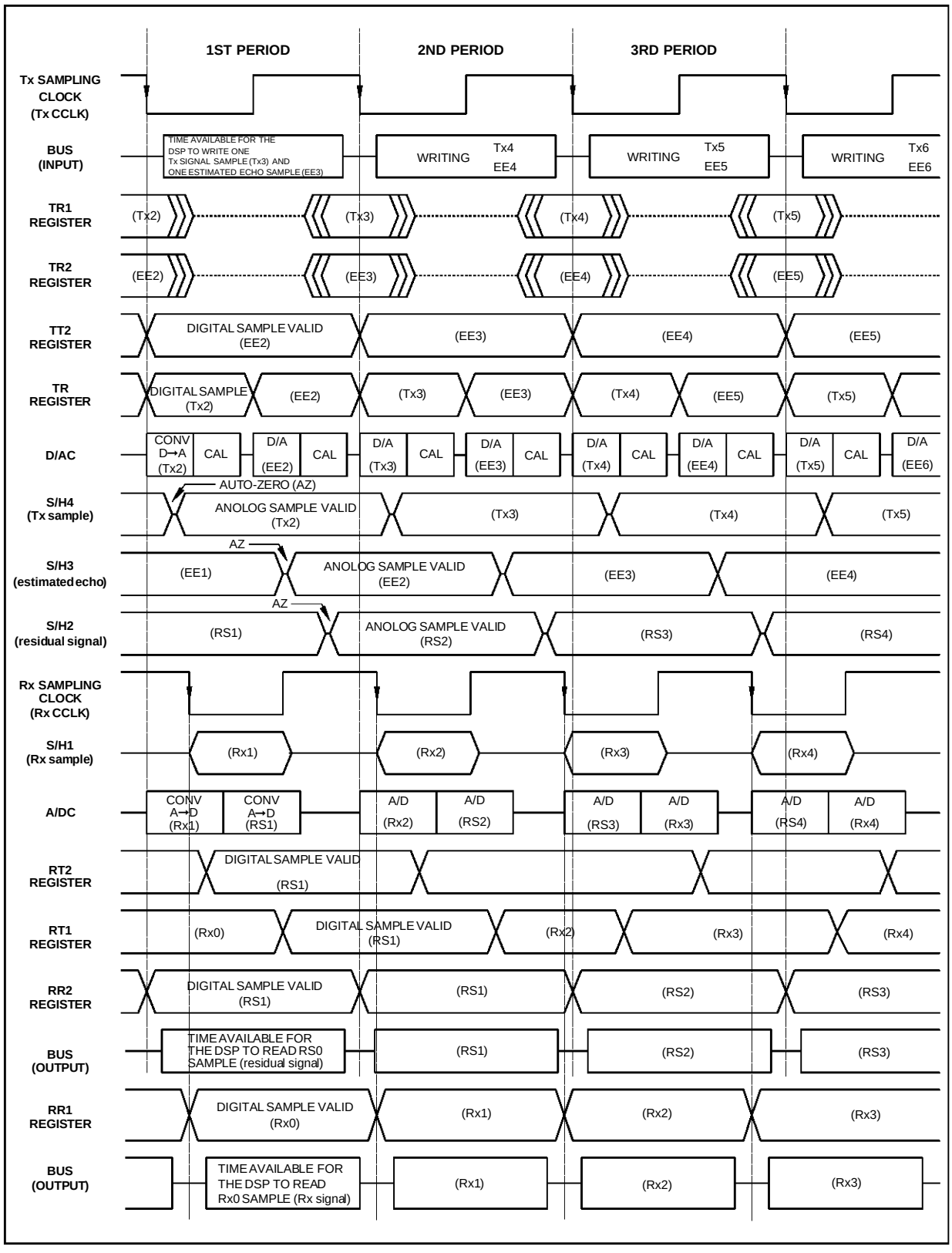
CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								ARC Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1	-	0	0	1
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR	-	-	0	0	1
RC3	68951	HP2	HP1	LP2	LP1	REJ	S/A	REC	-	0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1	-	EM2	EM1		0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1	-	-		1	0	0
RC6	68951	GDS2	GDS1	HDS	-	-	-	-		1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1	-	-		1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT	-	-		1	1	1

68952-17.TBL

APPENDIX 4

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



APPENDIX 5

FURTHER REFERENCES

Mafe Characterization Report

This report gives the results of the measurements performed on the TS68950-51-52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950. i.e the echo path and the Tx signal path. Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951.

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface.

Mafe Evaluation Board

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

The MAFE evaluation board is equipped with the TS68950/51/52 chip set and a phone line interface facilities.

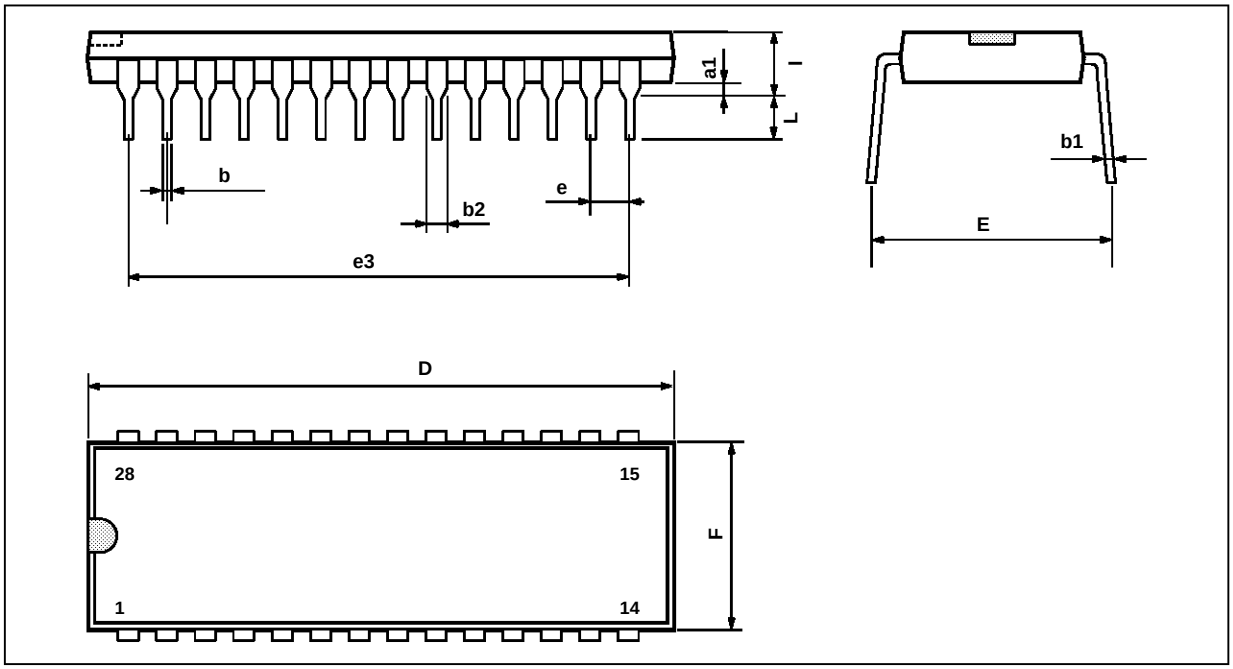
It can be directly connectable to an external Digital Signal Processor through a 50-pins connector or can be linked to the SGS-THOMSON family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

Application Note

This application note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



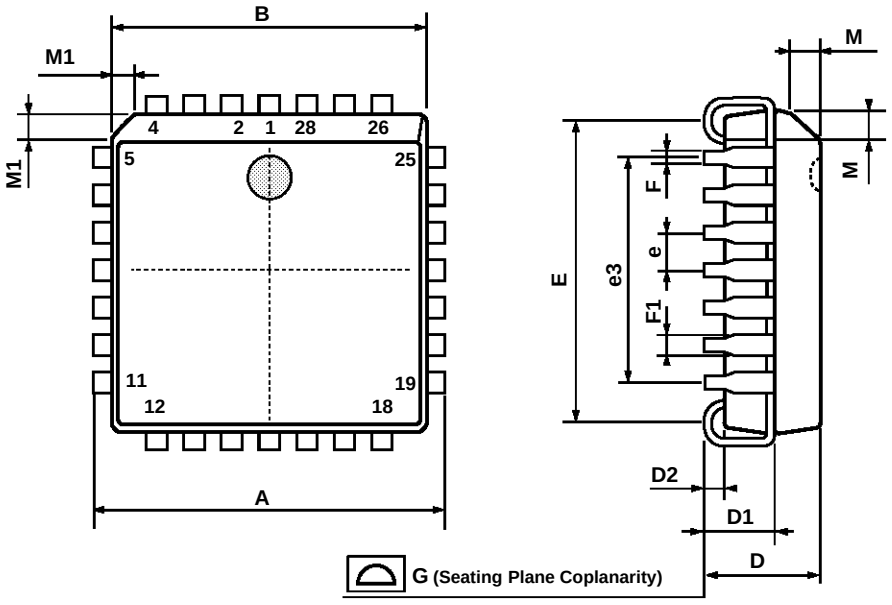
PM-DIP28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP28.TBL

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC LEADLESS CHIP CARRIER



PMPLCC28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

PLCC28.TBL